REMARKS

The application has been reviewed in light of the Office Action dated May 21, 2007. Claims 1-20 were pending. By this Amendment, new dependent claim 21 has been added. Accordingly, claims 1-21 are now pending, with claims 1, 10 and 19 being in independent form.

Claims 1 and 10 were rejected under 35 U.S.C. § 102(b) as purportedly anticipated by U.S. Patent No. 5,758,191 to Kasebayashi et al. Claims 2, 3, 9, 11, 12 and 18 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi in view of U.S. Patent No. 6,799,242 to Tsuda et al. Claims 4-6 and 13-15 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi in view of Tsuda and further in view of U.S. Patent No. 6,470,439 to Yamada et al. Claims 7, 8, 16 and 17 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi in view of Tsuda and Yamada and further in view of U.S. Patent No. 6,502,159 to Chuang. Claims 19 and 20 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over Kasebayashi in view of Tsuda and further in view of U.S. Patent No. 6,631,469 to Silvester.

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claims 1, 10 and 19 are patentable over the cited art, for at least the following reasons.

The present application relates to various improvements devised by applicant for data transfer (for example, by an optical disk drive device) with a host computer.

For example, claim 1 is directed to a communications interface apparatus comprising (a) a register circuit storing data to be transferred to a host computer, (b) a first memory storing first information indicating a specific address of the register circuit and representing an access to the communications interface apparatus executed by the host computer for a data transfer, (c) a

second memory ***storing second information, sent in association with the first information stored in the first memory and corresponding to said data to be transferred to said host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory***, and (d) a control circuit configured to perform an information writing operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed, in connection with said data to be transferred to said host computer.

Kasebayashi, as understood by Applicant, proposes an approach, in a magnetic disk drive, for managing a buffer having an area for storing burst data and another area for storing data in connection with write and read commands. In the system proposed by Kasebayashi, buffer 11 temporarily stores data exchanged between the magnetic disk apparatus and the host system 10, and has a burst area and a read/write area, address storage unit 12 stores address information representing addresses at which the burst area and the read/write area are set in the buffer 11 (that is, the locations in the buffer occupied by the burst area and the read/write area), and magnetic disk 13 is a recording medium of the magnetic disk apparatus. In addition, read unit 14 controls the address information stored in the address storage unit 12 in response to a read command sent from the host system 10, reads data required by the host system 10 from the magnetic disk 13, and writes the data in the read/write area indicated by the address information.

The Office Action equates the read unit 14 in the system proposed by Kasebayashi with the second memory and the control circuit in the communications interface apparatus of claim 1 of the present application.

The Office Action (page 14) states as follows:

Regarding Claims 1 and 10. Applicant argues that "Kasebayashi does not discloses or suggest a second memory storing second information, sent in association with the first information stored in the first memory and corresponding to said data to be transferred to said host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory". The examiner respectfully disagrees. Contrary to Applicant's argument, read section 14 does in fact teach these limitations, see Column 5, lines 57-61. It can be seen that the read unit 14 actively reads data from magnetic disk 13 and separately writes this data to buffer 11 (using two distinct steps), which would indicate that memory internal to read section 14 is necessarily present.

However, the read unit 14 in the system proposed by Kasebayashi, contrary to the contention in the Office Action, does not store data from the magnetic disk 13.

Fig. 3 of Kasebayashi is reproduced below:

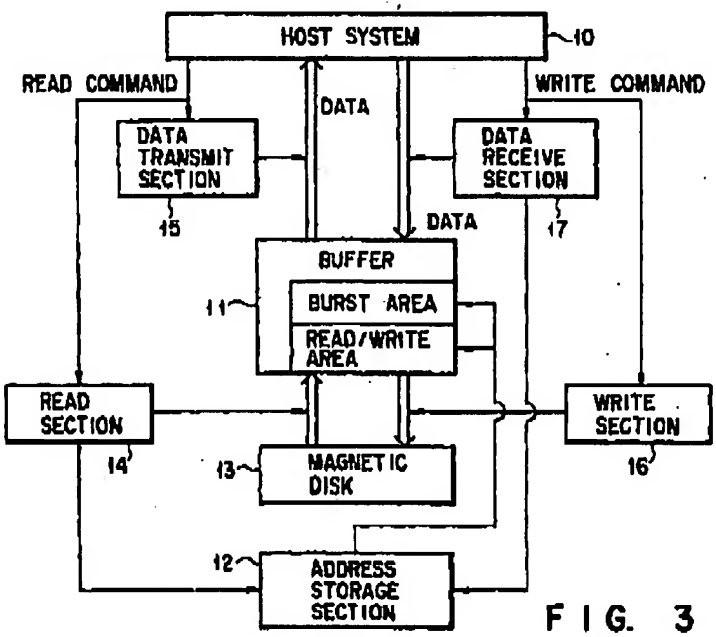


FIG. 3

It can be seen clearly in Fig. 3 of Kasebayashi that the data from the magnetic disk 13 flows directly to the buffer 11. In addition, there are no arrows indicating flow of data from the magnetic disk 13 to the read section 14. On the other hand, the read unit 14 does control flow of

the data from the magnetic disk 13 directly to the buffer 11, and thus in essence reads data from the magnetic disk 13, and writes the data in the buffer 11.

However, contrary to the contention in the Office Action, it is **not necessary** that the read section 14 of Kasebayashi have an internal memory. As noted above, the data flows directly from the magnetic disk 13 to the read section 14, albeit under control of the read section 14.

Further, contrary to the contention in the Office Action, the address information stored in the address storage unit 12 of Kasebayashi does not correspond to the data to be transferred to the host computer.

As discussed in Kasebayashi, column 6, lines 14-54, and shown in Figs. 4 and 5 of Kasebayashi, the address storage unit 12 stores information indicating the locations in buffer 11 of segments A (area for read and write operations) and B (burst area). That is, the information stored in the address storage unit 12 are the start and end addresses for each of the sections A and B.

However, the address storage unit 12 of Kasebayashi does not store specific addresses corresponding to the data to be transferred to the host computer (that is, with each address indicating a buffer location into which a corresponding data is to be written).

Kasebayashi simply does not teach or suggest a communications interface apparatus comprising a register circuit, a first memory, a second memory and a control circuit, wherein the second memory ***stores second information, sent in association with the first information (indicating a specific address of the register circuit) stored in the first memory and corresponding to said data to be transferred to said host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory***, as provided by the subject matter of claim 1 of the present application.

The other cited references do not cure the deficiencies of Kasebayashi.

Tsuda, as understood by Applicant, proposes an optical disc player that enters a sleep mode when it is inactive for a predetermined time. Fig. 7 of Tsuda shows a digital signal processor 250, a CD-ROM decoder 260, control microcomputer 244, a clock generator 62 and a buffer RAM 7 which collectively are proposed by Tsuda to be used in an optical disc player.

Tsuda, column 8, lines 11-25, states as follows:

> Recovery to a normal operational mode from the sleep mode will now be described. When a recovery command to the normal operational mode is supplied from the host computer to the microcomputer interface 233, the recovery command is transferred from the microcomputer interface 233 to the control microcomputer 244, which responds to the recovery command to deliver a stop termination command to the clock generating circuit 62, which in turn supplies a clock signal to the various circuits. In addition, the control microcomputer 244 delivers a TOC transfer command to the memory control circuit 61, which then reads the TOC data stored in the address register 230 from the SRAM 56 beginning with the first address, and writes such TOC data into the buffer RAM 7 via the microcomputer interface 233 and the memory control circuit 232.

Thus, in the approach proposed by Tsuda, when a recovery command (to return to normal mode from sleep mode) is received from a host computer, the recovery command is transferred from the microcomputer interface 233 to the control microcomputer 244, the control microcomputer 244 in turn sends a transfer command to memory control circuit 61, and the memory control circuit 61 then reads TOC data stored in address register 230 and writes the TOC data into buffer RAM 7. The TOC data is used by the optical disc player proposed by Tsuda and is not transferred to the host computer.

Yamada, as understood by Applicant, proposes a FIFO (first-in-first-out) memory control circuit, for performing asynchronous read/write control in an electronic device, when a write clock and a read clock are different.

Chuang, as understood by Applicant, proposes an approach for improving data

throughput in a computer system including control circuitry responsive to signals from a CPU which specify whether data from a CD-ROM is to be sent directly to a MPEG decoder circuit or to be sent to system memory.

However, Tsuda, Yamada and Chuang, like Kasebayashi, do not teach or suggest a second memory ***storing second information, sent in association with the first information (indicating a specific address of the register circuit) stored in the first memory and corresponding to said data to be transferred to said host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory***, as provided by the subject matter of claim 1 of the present application.

Applicant simply does not find teaching or suggestion in the cited art of a communications interface apparatus comprising a register circuit, a first memory, a second memory and a control circuit, wherein the second memory stores second information, sent in association with the first information stored in the first memory and corresponding to said data to be transferred to said host computer, to be written into the register circuit at the specific address indicated by the first information stored in the first memory, as provided by the subject matter of claim 1 of the present application.

Independent claim 10 is patentably distinct from the cited art for at least similar reasons.

Accordingly, Applicant respectfully submits that independent claims 1 and 10, and the claims depending therefrom, are patentable over the cited art.

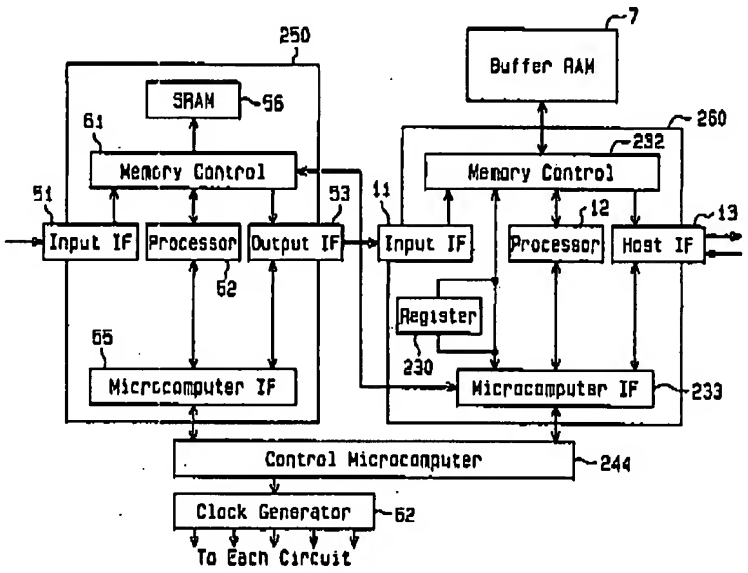
Regarding independent claim 19 directed to an optical disk drive apparatus, Kasebayashi is simply not relevant to the subject matter of claim 19 of the present application since Kasebayashi is concerned with buffer management in the transfer of data between a magnetic hard disk and a host computer, and is not concerned with an optical disk drive apparatus. One

skilled in the art would not have been motivated to apply the teachings of Kasebayashi in connection with the subject matter of claim 19 of the present application or to combine Kasebayashi with Tsuda, since Kasebayashi is simply not relevant to an optical disk drive apparatus.

Tsuda does not teach or suggest various features of claim 19.

For example, in the signal processing circuit shown in Fig. 7 of Tsuda (reproduced below), a clock generator 62 is provided for generating clock signals to be supplied to various circuits in the optical disk player.

Fig.7



On the other hand, the clock generator 62 is not configured to supply the clock signals at all to the host interface 13 (which provides an interface for the optical disk player to communicate with the host computer) or other parts of data processing circuit 260.

In addition, the clock generator 62 stops generating clock signals when the player enters sleep mode. It is clear from Tsuda, column 8, lines 11-25, which was cited in the Office Action,

that the interface 13 remains active while the remainder of the optical disk player enters the sleep mode.

Applicant does not find teaching or suggestion in Tsuda, however, of an optical disk drive apparatus comprising, amongst other elements, an interface circuit for interfacing communications between the optical disk drive mechanism and a host computer, the interfacing circuit comprising a clock generator configured to generate ***a clock signal with which the data processor performs the predetermined data processing operation***, and an operation mode changer configured to control the clock generator to reduce a frequency of the clock signal to a value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode, as provided by the subject matter of claim 19 of the present application.

Silvester, as understood by Applicant, proposes an approach for managing a sleep mode in a computer system, wherein in sleep mode, a wakeup alarm is triggered in the computer system according to a user-specified periodic interval, and in response to the wakeup alarm, the computer system automatically exits the sleep mode and enters a wake mode, and then automatically exchanges data, such as email, with a host and returns to the sleep mode.

However, Silvester is concerned with a sleep mode in a computer system and not with an optical disk drive apparatus. Therefore, Silvester is not relevant to the subject matter of claim 19 of the present application. One skilled in the art would not have been motivated to apply the teachings of Silvester in connection with the subject matter of claim 19 of the present application or to combine Silvester with Tsuda, since Silvester is simply not relevant to an optical disk drive apparatus.

Neither Silvester nor Tsuda (nor Kasebayashi) teaches an optical disk drive apparatus

comprising, amongst other elements, an interface circuit for interfacing communications between the optical disk drive mechanism and a host computer, the interfacing circuit comprising a buffering circuit block configured to buffer data received through an input terminal, the buffering circuit block including a first data transfer path configured to transfer the data received through the input terminal to the data processor not via a memory, and a second data transfer path configured to transfer the data received through the input terminal to the data processor via a memory, and a path selection controller configured to control the buffering circuit block to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode, in the optical disk drive apparatus, as provided by the subject matter of claim 19 of the present application.

Further, Silvester, like Tsuda, does not teach or suggest an optical disk drive apparatus comprising, amongst other elements, an interface circuit for interfacing communications between the optical disk drive mechanism and a host computer, the interfacing circuit comprising a clock generator configured to generate ***a clock signal with which the data processor performs the predetermined data processing operation***, and an operation mode changer configured to control the clock generator to reduce a frequency of the clock signal to a value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode, as provided by the subject matter of claim 19 of the present application.

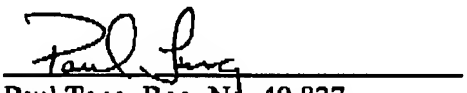
Accordingly, Applicant respectfully submits that independent claim 19 and claims depending therefrom are patentable over the cited art.

In view of the remarks hereinabove, Applicant submits that the application is now in condition for allowance. Accordingly, Applicant earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Patent Office is hereby authorized to charge any fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,



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